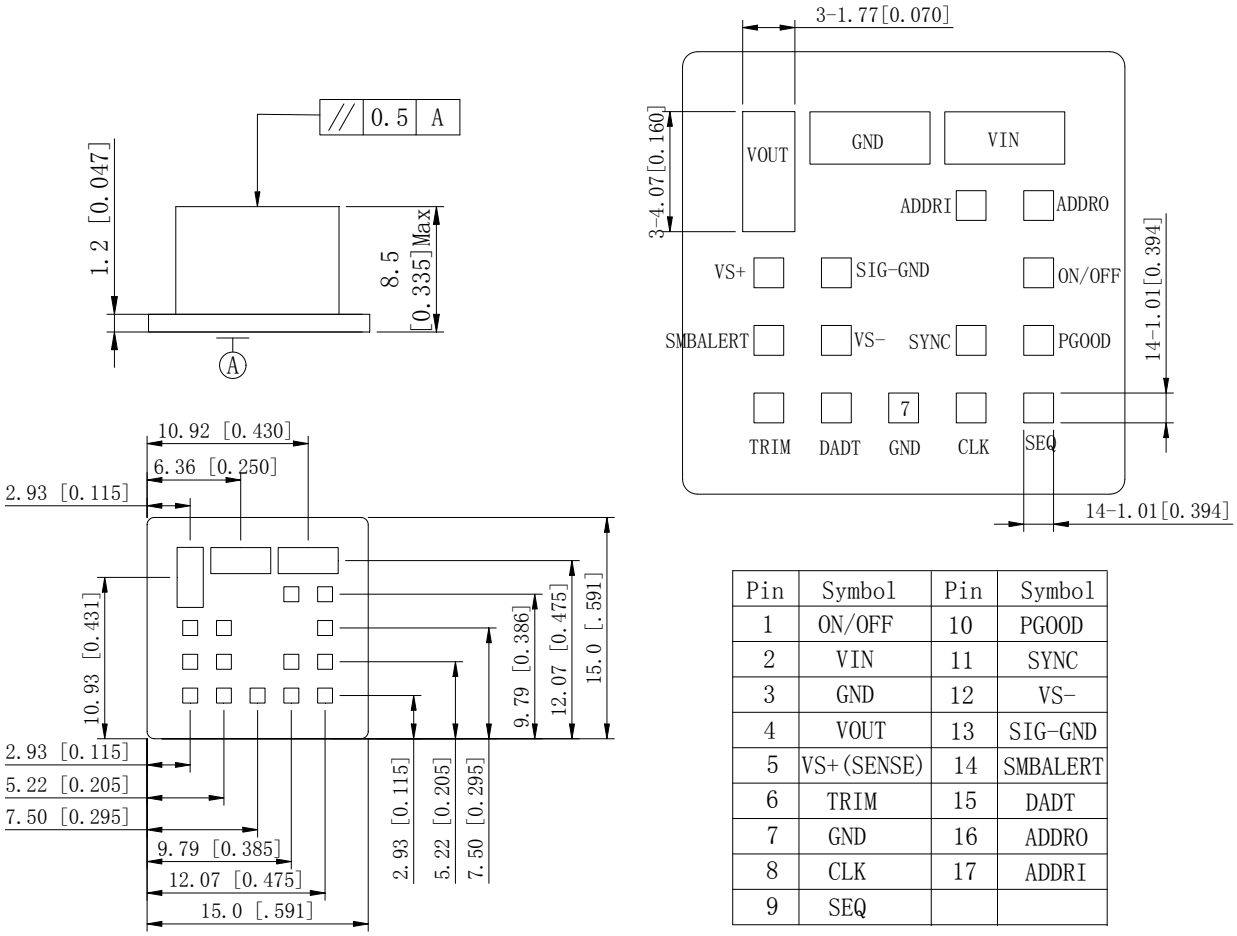
DC/DC ZBU12-12BS

Input 3V～14.4V output 0.45V～5.5V/12A Digital Power

Features

- *Size :15mm×15mm×8.5mm*
- *Digital interface through the PMBus™# protocol*
- *Output voltage programmable from 0.6Vdc to 5.5Vdc via external resistor. Digitally adjustable down to 0.45Vdc*
- *Flexible output voltage sequencing EZ-SEQUENCE\Power Good signal\Fixed switching frequency with capability of external synchronization*
- *High efficiency: typical 94% (12V input,5V output)*
- *Remote enable control（low level or float on）*
- *Input undervoltage protection\Output overcurrent protection (non-latching)\Overtemperature protection*
- *-40℃～+85℃ ambient temperature*

Outline



Pin	Symbol	Pin	Symbol
1	ON/OFF	10	PGOOD
2	VIN	11	SYNC
3	GND	12	VS-
4	VOUT	13	SIG-GND
5	VS+(SENSE)	14	SMBALERT
6	TRIM	15	DADT
7	GND	16	ADDRO
8	CLK	17	ADDRI
9	SEQ		

Notes:all dimensions in mm(inches)
Tolerances:
X.X±0.5mm(X.XX±0.02)
X.XX±0.25mm(X.XXX±0.010)

Specification

Unless otherwise specified, all values are given at: 25℃, one standard atmosphere pressure, pure resistive load and basic connection; Input filter:one 47μF aluminum electrolytic capacitor and two 22μF ceramic capacitances; output 22μF ceramic capacitance.

Input		Symbol	Min	Typ	Max	Unit	Conditions
Input Voltage		V_{in}	3	12.0	14.4	V	$V_O \leq 1.2V$
			3.5	12.0	14.4	V	$1.2V < V_O \leq 1.8V$
			4.5	12.0	14.4	V	$1.8V < V_O \leq 3.3V$
			6.0	12.0	14.4	V	$V_O > 3.3V$
No-Load Input Current		$I_{in,nl}$	–	50	–	mA	Vin=12V,V_O=0.6V，I_O=0A
			–	85	–		Vin=12V,V_O=5V，I_O=0A
Negative Logic Remote Control	OFF	–	2	–	Vin	V	Refer to GND;
	ON	–	0	–	0.6	V	Refer to GND ; Turn on when CNT floating.
Under Voltage Protection	Under Voltage Threshold	V_{UVLO}	2.25	–	3.025	V	Initial Settings
	Under Voltage Protection Hysteresis	$\triangle V_{UVLO}$	–	0.25	–	V	
	Adjustable Under Voltage Threshold	–	2.5	–	14	V	PMBus
	Resolution of Under Voltage Threshold	–	–	–	500	mV	

Output		Symbol	Min	Typ	Max	Unit	Conditions
Output Voltage	Adjustment range	V_O	0.6	–	5.5	V	selected by an external resistor
	Adjustment range	$V_{O,\ adj}$	-25	–	+25	$\%V_O$	PMBus
	Adjustment Step Size	–	0.4	–	–	$\%V_O$	
Output Current		I_O	0	–	12	A	—
Line Regulation		S_V	–	–	±5	mV	$V_O < 2.5V$
			–	–	±0.4	$\%V_O$	$V_O \geq 2.5V$
Load Regulation		S_I	–	–	±10	mV	—
Output Over Current Protection Range		$I_{O,lim}$	14	19	21	A	Vin=12V, Continuous operation under this condition is not recommended
Peak to Peak Ripple and Noise		$\triangle V_{PP}$	–	–	120	mV	20 MHz,22μF ceramic capacitance applied at output
Output Short-circuit Protection		–	Hiccup mode, automatic recovery				—
Rise Time		T_{rise}	–	2.5	4	ms	$I_{O,nom}$，Resistance load
Output delay time		T_{delay}	–	1.5	3	ms	$I_{O,nom}$，Resistance load
Output Overshoot		V_{TO}	–	–	3	$\%V_O$	—
Capacitive Load		C_O	22	–	47	μF	Loop adjustment function is not utilized,ESR≥1mΩ
			22	–	1000	μF	ESR≥0.15mΩ Loop

		22	–	5000	μF	ESR≥10mΩ	adjustment function is utilized

Continue

Output		Symbol	Min	Typ	Max	Unit	Conditions
Load Transient	Recovery Time	t_{tr}	–	20	50	μs	50%～100% load step change;di/dt:2.5A/μs
	Voltage Deviation	$\triangle V_{tr}$	–	±60	±120	mV	
Overvoltage threshold for PGOOD ON		–	–	108	–	%V_O	Signal Interface Open Drain, V_{supply} ≤5V
Overvoltage threshold for PGOOD OFF		–	–	110	–		
Undervoltage threshold for PGOOD ON		–	–	92	–		
Undervoltage threshold for PGOOD OFF		–	–	90	–		
Pulldown resistance of PGOOD pin		–	–	–	50	Ω	
Sink current capability into PGOOD pin		–	–	–	5	mA	
Tracking Accuracy	Power-Up:2V/ms	V_{SEQ} -V_O	–	–	100	mV	—
	Power-Down:2V/ms	V_{SEQ} -V_O	–	–	100	mV	

Digital Interface Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
PMBus Signal Interface Characteristics						
Input High Voltage (CLK, DATA)	V_{IH}	2.1	–	3.6	V	—
Input Low Voltage (CLK, DATA)	V_{IL}	–	–	0.8	V	—
Input high level current (CLK, DATA)	I_{IH}	-10	–	10	μA	—
Input low level current (CLK, DATA)	I_{IL}	-10	–	10	μA	—
Output Low Voltage (CLK, DATA, SMBALERT#)	V_{OL}	–	–	0.4	V	I_{OUT}=2mA
Output high level open drain leakage current (DATA,SMBALERT #)	I_{OH}	0	–	10	μA	V_{OUT}=3.6V
Pin capacitance	C_O	–	0.7	–	pF	—
PMBus Operating frequency range	F_{PMB}	10	–	400	KHz	Slave Mode
Data hold time	$t_{HD;\ DAT}$	0/300	–	–	ns	Receive Mode/Transmit Mode
Data setup time	$t_{SU;\ DAT}$	250	–	–	ns	—
Measurement System Characteristics						
Read delay time	t_{DLY}	153	192	231	μs	—
Output current measurement range	I_{RNG}	0	–	21	A	—

Output current measurement resolution	I_{RES}	62.5	–	–	mA	—

Continue

Digital Interface Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Output current measurement gain accuracy at 25°C	I_{ACC}	–	–	±5	%	—
Output current measurement offset	I_{OFST}	–	–	0.1	A	—
V_{OUT} measurement range	$V_{OUT(rng)}$	0	–	5.5	V	—
V_{OUT} measurement resolution	$V_{OUT(res)}$	–	15.625	–	mV	—
V_{OUT} measurement accuracy	$V_{OUT(ACC)}$	-15	–	15	%	—
V_{OUT} measurement offset	$V_{OUT(ofst)}$	-3	–	3	%	—
V_{IN} measurement range	$V_{IN(rng)}$	3	–	14.4	V	—
V_{IN} measurement resolution	$V_{IN(res)}$	–	32.5	–	mV	—
V_{IN} measurement accuracy	$V_{IN(ACC)}$	-15	–	15	%	—
V_{IN} measurement offset	$V_{IN(ofst)}$	-5.5	–	1.4	LSB	—

General		Symbol	Min	Typ	Max	Unit	Conditions
Efficiency		η	93	94	–	%	V_{in}=12V,12A,V_O=5.0V
			89	91	–	%	V_{in}=12V,12A,V_O=2.5V
			83	84	–	%	V_{in}=12V,12A,V_O=1.2V
			74	75	–	%	V_{in}=12V,12A,V_O=0.6V
			70	71	–	%	V_{in}=12V,12A,V_O=0.45V
Switching Frequency		f_s	–	600	–	kHz	—
Frequency Synchronization	Synchronization Frequency range	f_s	510	–	720	kHz	—
	Input High Voltage	V_{IH}	2.0	–	–	V	—
	Input High Voltage	V_{IH}	2.0	–	–	V	—
	Input Low Voltage	V_{IL}	–	–	0.4	V	—
	Input Current,SY-NC	I_{SYNC}	–	–	100	nA	—
	Minimum Pulse Width,SYNC	t_{SYNC}	100	–	–	ns	—
	Maximum SYNC Rise Time	$t_{SYNC-SH}$	100	–	–	ns	—
Operating Ambient Temperature		–	-40	–	85	℃	See Derating Curve
MTBF		–	5×10^6	–	–	h	BELLCORE TR-332
Storage Temperature		–	-55	–	125	℃	—
Relative Humidity		–	10	–	90	%	40℃±2℃，No ondensing
Temperature Coefficient		S_T	–	–	±0.02	%/℃	—

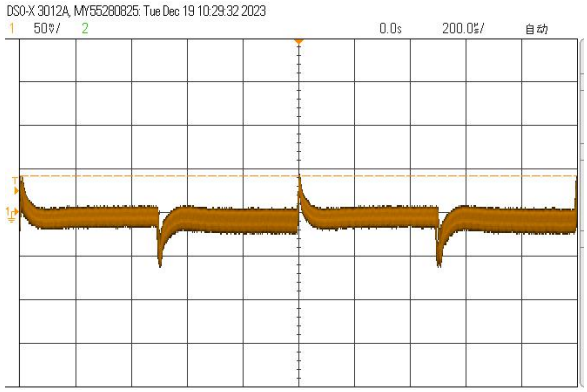
Over Temperature Protection threshold	T_{ref}	–	120	–	℃	See Below for Specific Test Points

Continue

General	Symbol	Min	Typ	Max	Unit	Conditions
Hand Soldering	Maximum soldering Temperature < 425℃,and duration < 5s					
Wave Soldering	Maximum soldering Temperature < 255℃,and duration < 10s					
Weight	–	–	3	–	g	—

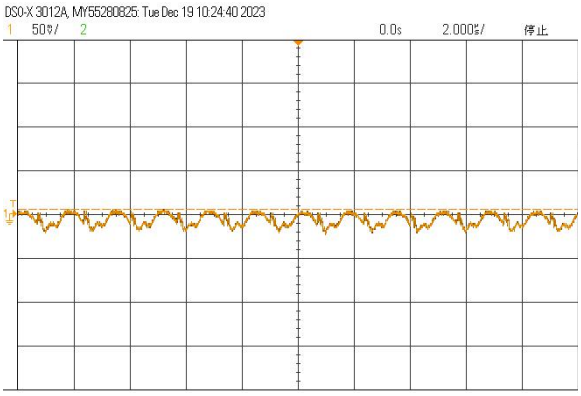
Characteristic Curves（V_O=0.6V）

Load Transient Response



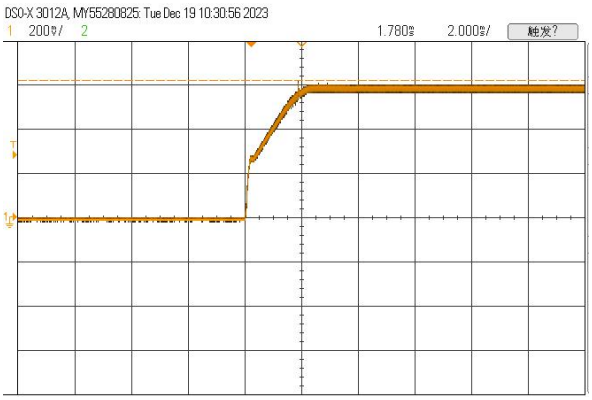
50%～100%～50% load, 2.5A/μs,Vin=12Vdc

Output Ripple and noise



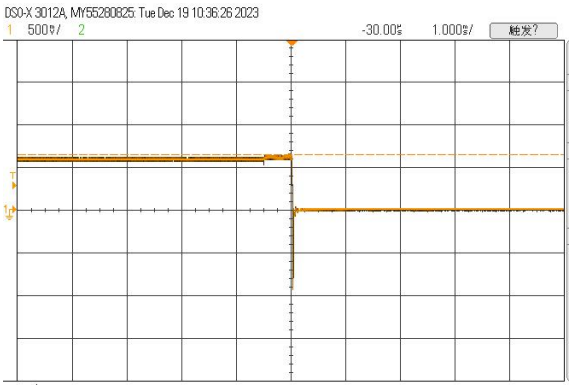
Vin=12Vdc,Io=12A

Output rise time



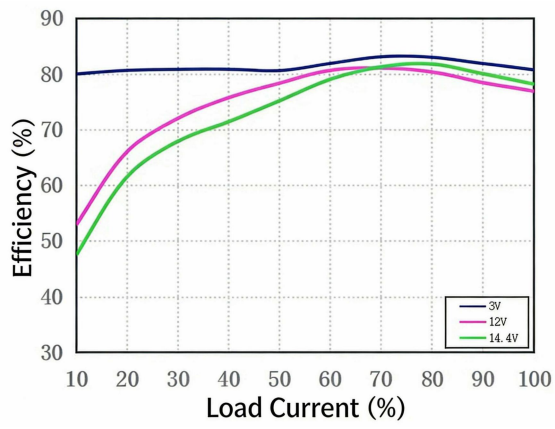
Vin=12Vdc,Io=12A

Power-Down Characteristics

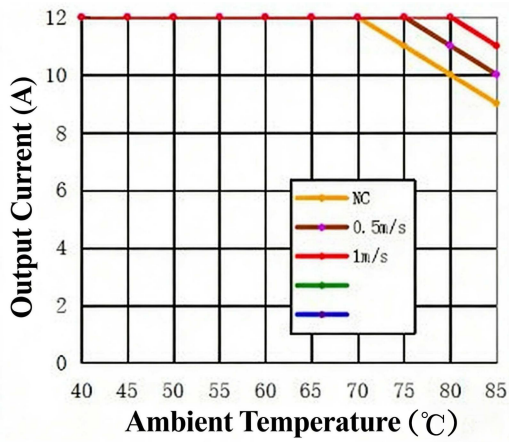


Vin=12Vdc,Io=12A

Efficiency vs Io & Vin

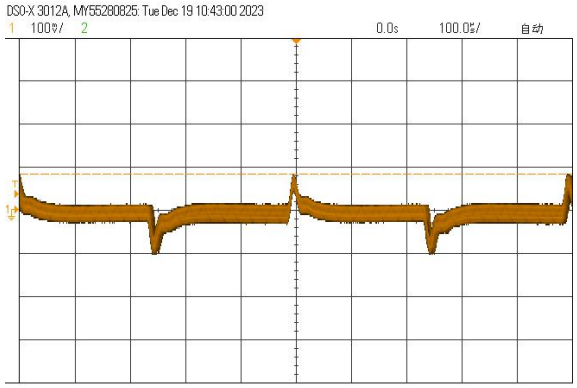


Derating（Vin=12Vdc）



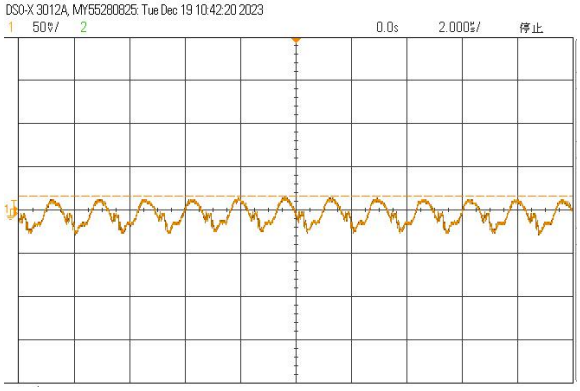
Characteristic Curves（Vo=1.2V）

Load Transient Response



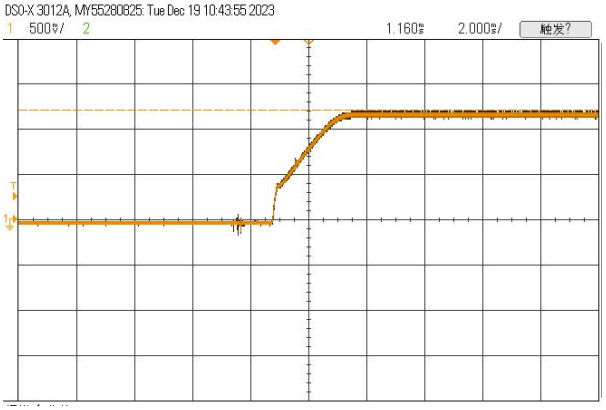
50%～100% load, 2.5A/μs
Vin=12Vdc

Output Ripple and noise



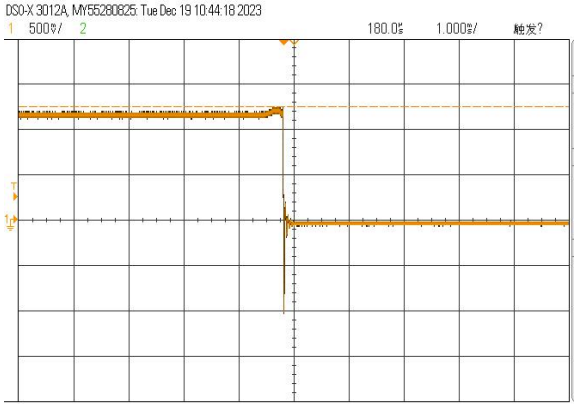
Vin=12Vdc,Io=12A

Output rise time



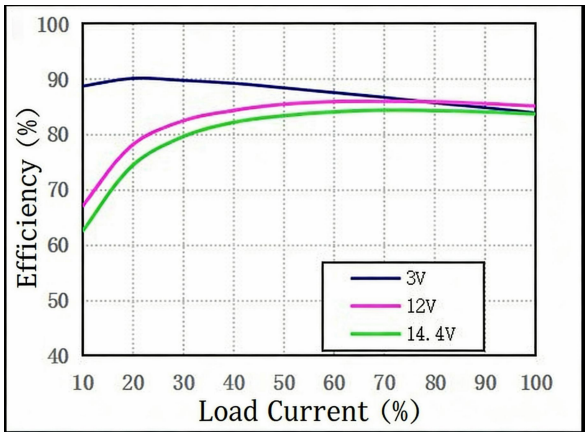
Vin=12Vdc,Io=12A

Power-Down Characteristics

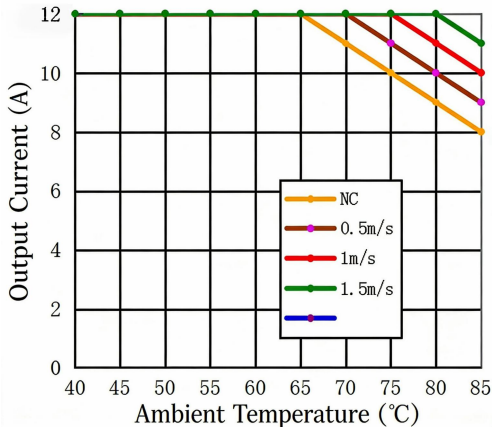


Vin=12Vdc,Io=12A

Efficiency vs Io & Vin

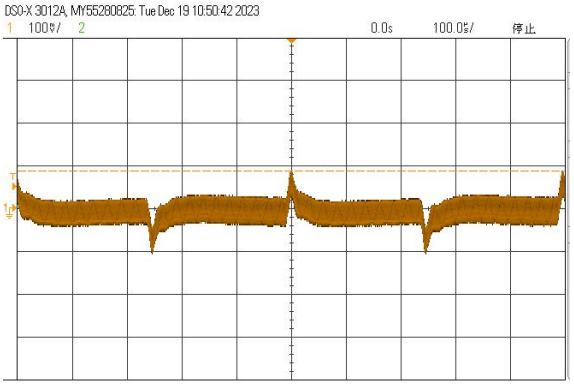


Derating（Vin=12Vdc）



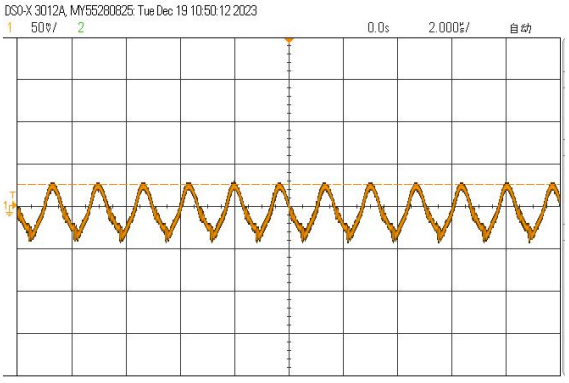
Characteristic Curves（Vo=2.5V）

Load Transient Response



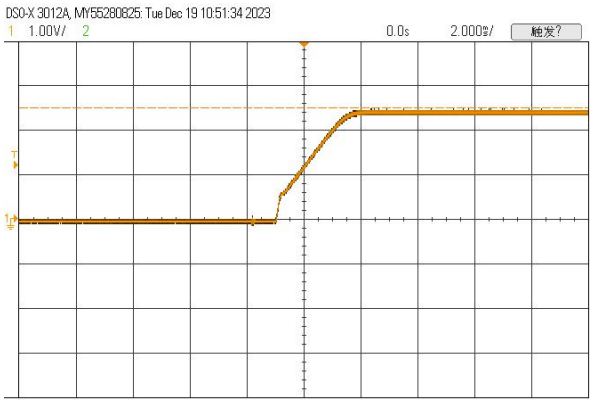
50%～100% load, 2.5A/μs
Vin=12Vdc

Output Ripple and noise



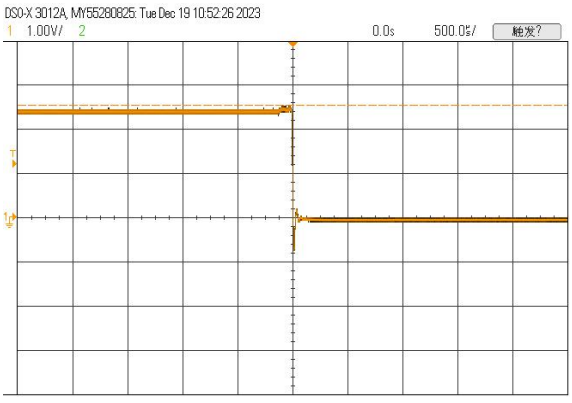
Vin=12Vdc,Io=12A

Output rise time



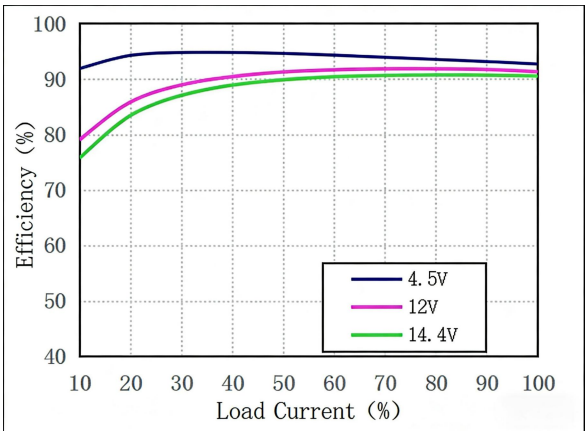
Vin=12Vdc,Io=12A

Power-Down Characteristics

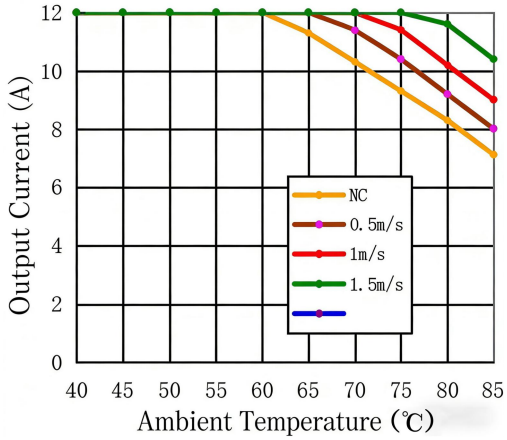


Vin=12Vdc,Io=12A

Efficiency vs Io & Vin

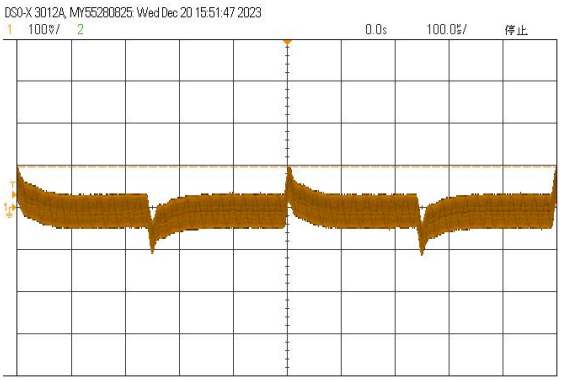


Derating（Vin=12Vdc）



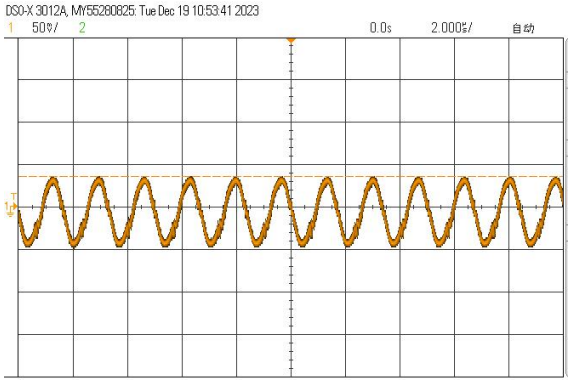
Characteristic Curves（Vo=5V）

Load Transient Response



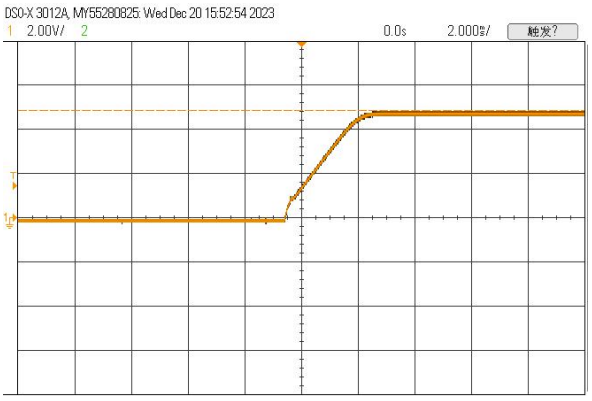
50%～100%load, 2.5A/μs
Vin=12Vdc

Output Ripple and noise



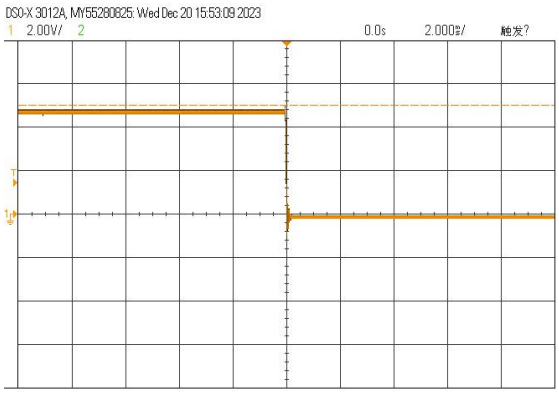
Vin=12Vdc,Io=12A

Output rise time



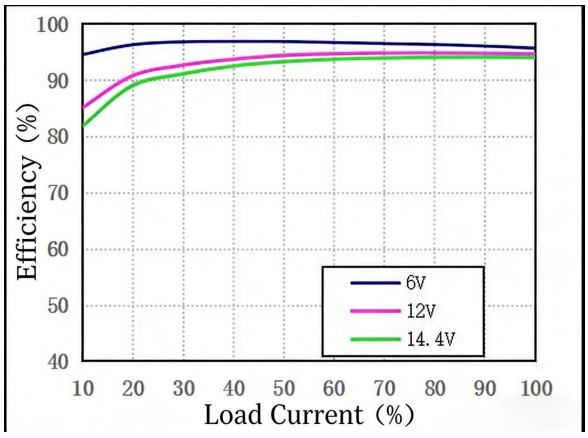
Vin=12Vdc,Io=12A

Power-Down Characteristics

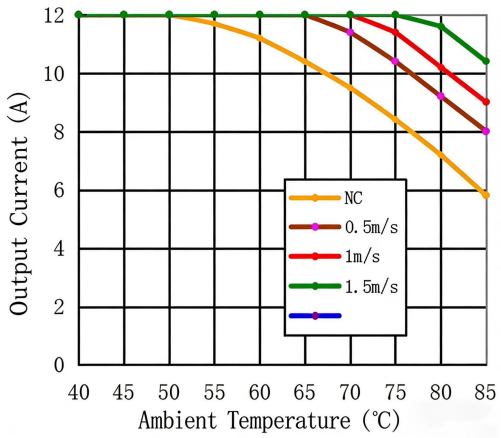


Vin=12Vdc,Io=12A

Efficiency vs Io & Vin



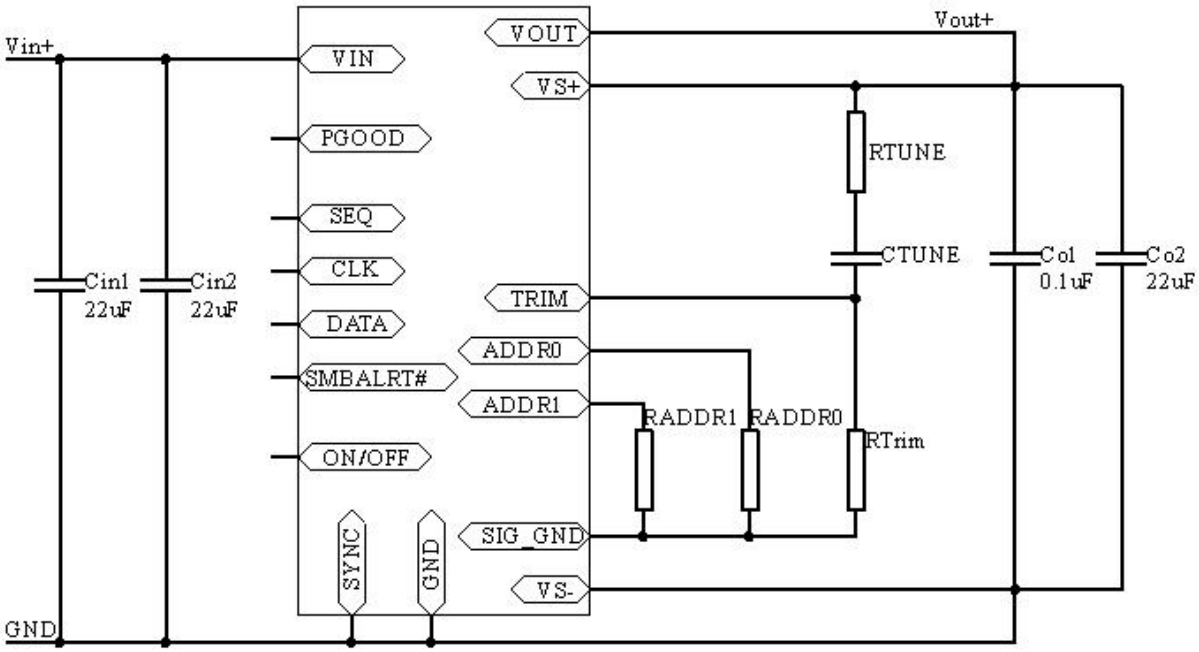
Derating（Vin=12Vdc）



Design Considerations

Basic

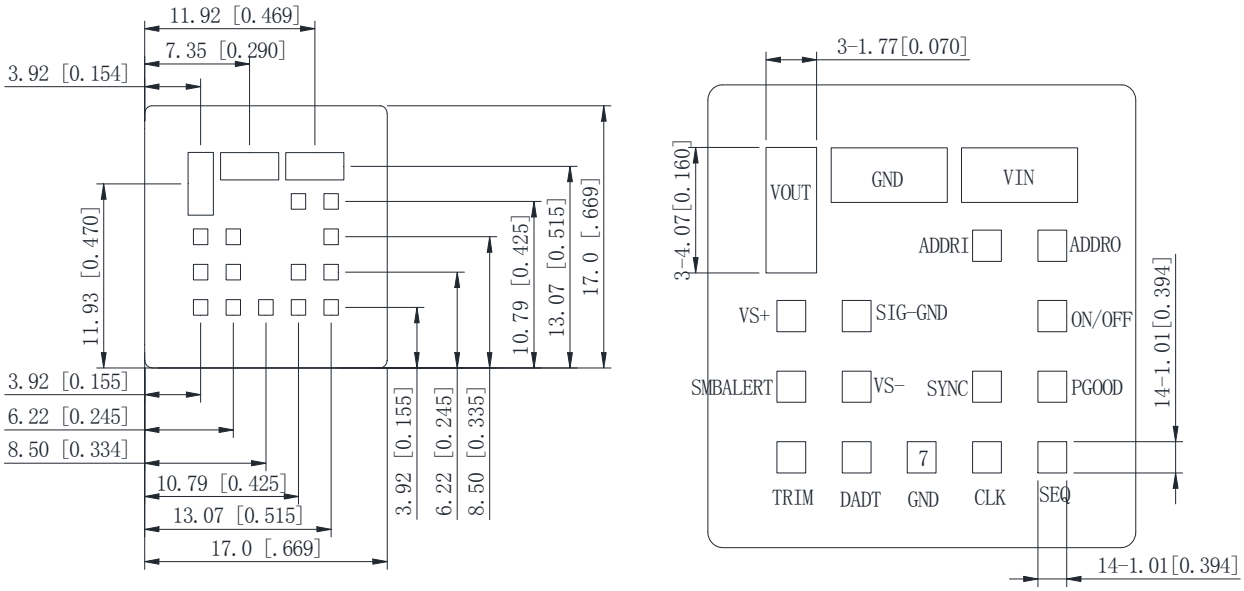
Connection



Notes: The DATA, SMBALRT, and CLK pins have no internal pull-up resistors. Pull-ups and drive source are typically provided by the SMBus controller. This figure shows only the basic conditions for normal rated output voltage and power. Please refer the instruction followed for further information.

Recommended

Layout



Input Voltage Range

The input voltage range of the DC/DC converter is 3V to 14.4V.The input impedance of the converter looks like a negative resistor, which can interact with the reactance of the power bus (including any filter elements that have been added to the input of the converter), causes an unstable condition. Depending on

the internal transformer's impedance, the external impedance usually should not exceed the 10% of the internal. So, the source impedance of the Power bus should be kept as low as possible.

Remote Control

The module can be turned ON and OFF either by using the ON/OFF pin (Analog interface)or through the PMBus interface(Digital). The module can be configured in a number of ways through the PMBus interface to react to the two ON/OFF inputs:

Module ON/OFF can be controlled only through the analog interface (digital interface ON/OFF commands are ignored).There are two types of logic states: positive logic and negative logic. In positive logic control, applying a high level or leaving the ON/OFF pin floating turns the module on, and applying a low level to the ON/OFF pin turns the module off. In negative logic control, applying a low level or leaving the ON/OFF pin floating turns the module on, and applying a high level to the ON/OFF pin turns the module off. This product uses negative logic control.

Module ON/OFF can be controlled only through the PMBus interface (analog interface is ignored)

Module ON/OFF can be controlled by either the analog or digital interface.

The default state of the module (as shipped from the factory)is to be controlled by the analog interface only. If the digital interface is to be enabled, or the module is to be controlled only through the digital interface, this change must be made through the PMBus. These changes can be made and written to non-volatile memory on the module so that it is remembered for subsequent use.

External Capacitance

At least 2×22 ceramic capacitors must be placed directly adjacent to the input pin of the module, to minimize input ripple voltage and ensure module stability.

These modules are designed for low output ripple voltage and will meet the maximum output ripple specification with 0.1μF ceramic and 22μF ceramic capacitors at the output of the module. However, additional output filtering may be required by the system designer for a number of reasons.First, there may be a need to further reduce the output ripple and noise of the module. Second, the dynamic response characteristics may need to be customized to a particular load step change.

To reduce the output ripple and improve the dynamic response to a step load change, additional capacitance at the output can be used. Low ESR polymer and ceramic capacitors are recommended to improve the dynamic response of the module. For stable operation of the module, limit the capacitance to less than the maximum output capacitance as specified in the electrical specification table. Optimal performance of the module can be achieved by using the Tunable Loop™ feature described later in this data sheet.

Tunable Loop™

The module has a feature that optimizes transient response of the module called Tunable Loop™.

External capacitors are usually added to the output of the module for two reasons: to reduce output ripple and noise and to reduce output voltage deviations from the steady-state value in the presence of dynamic load current changes. Adding external capacitance however affects the voltage control loop of the module, typically causing the loop to slow down with sluggish response.Larger values of external capacitance could also cause the module to become unstable.

The Tunable Loop™ allows the user to externally adjust the voltage control loop to match the filter network connected to the output of the module. The Tunable Loop™ is implemented by connecting a series R-C between the VS+and TRIM pins of the module. This R-C allows the user to externally adjust the voltage loop feedback compensation of the module.

Recommended values of RTUNE and CTUNE for different output capacitor combinations are given in Table 1. Table 2 shows the recommended values of RTUNE and CTUNE for different values of ceramic output capacitors up to 1000uF that might be needed for an application to meet output ripple and noise requirements. Selecting RTUNE and CTUNE according to Table 1 will ensure stable operation of the module. In applications with tight output voltage limits in the presence of dynamic current loading, additional output capacitance will be required. Table 2 lists recommended values of RTUNE and CTUNE in order to meet 2% output voltage deviation limits for some common output voltages in the presence of a 6A to 12A step change (50% of full load), with an input voltage of 12V.

Table 1						
Co	**1×47μF**	**2×47μF**	**4×47μF**	**6×47μF**	**10×47μF**	**20×47μF**
R_{TUNE}	330Ω	330Ω	330Ω	330Ω	330Ω	220Ω
C_{TUNE}	100pF	560pF	1500pF	2200pF	10nF	6800pF

Table 2						
Vo	5V	3.3V	2.5V	1.8V	1.2V	0.6V
Co	5×47μF	1×47μF +330μF Polymer	3×47μF +330μF Polymer	1×47μF +2×330μF Polymer	1×47μF +3×330μF Polymer	3×47μF +6×330μF Polymer
R_{TUNE}	330Ω	330Ω	270Ω	270Ω	220Ω	180Ω
C_{TUNE}	1500pF	2700pF	3300pF	5600pF	10nF	47nF

Note: The capacitors used in the Tunable Loop tables are 47μF/3mΩ ESR ceramic and 330μF/12mΩ ESR polymer capacitors.

Output Voltage Adjust

Resistive trim：

Change the Rtrim resistive， output voltage change from 0.6V to 5.5V.To calculate the value of the trim resistor, Rtrim for a desired output voltage,should be as per the following equation:

$$Rtrim = \frac{12}{(V_O - 0.6)} K\Omega$$

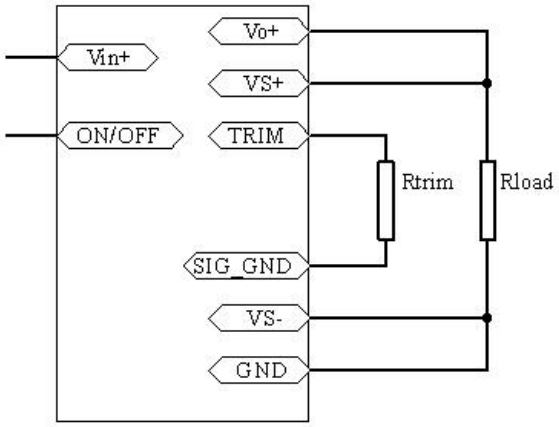


Table 3 External Resistor Value	
Output Voltage (V)	**Calculated Value (kΩ)**
0.6	**open**
0.9	**40**
1.0	**30**
1.2	**20**
1.5	**13.33**
1.8	**10**
2.5	**6.316**
3.3	**4.444**
5.0	**2.727**

Output Voltage Adjustment Using the PMBus

When PMBus commands are used to trim or margin the output voltage, the value of VREF is what is changed inside the module, which in turn changes the regulated output voltage of the module.

The nominal output voltage of the module can be adjusted with a minimum step size of 0.4% over a +25% range from nominal using the VOUT_TRIM command over the PMBus.The specific adjustment values are calculated using the following formula:

$$V_{ref} = (VOUT\_TRIM \times VOUT\_SCALE\_LOOP) + 0.6$$

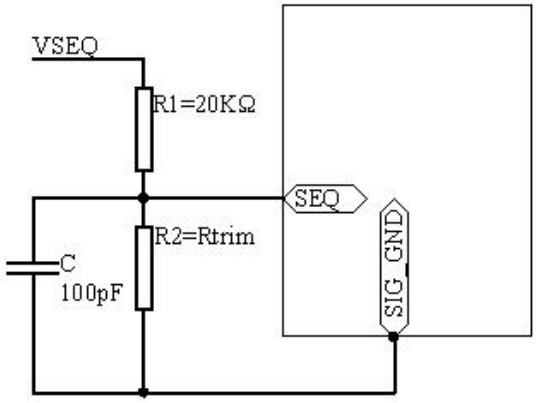
VOUT_SCALE_LOOP is 0.5,For example, to adjust V_{ref} to 0.45V, set the VOUT_TRIM command input to -0.3V.

Output Voltage Sequencing

The power module indudes a sequending feature, EZ-SEQUENCE that enables users to implement various types of output voltage sequencing in their applications. This is accomplished via an additional sequencing pin. When not using the sequencing feature, leave it unconnected.

The voltage applied to the SEQ pin should be scaled down by the same ratio as used to scale the output

voltage down to the reference voltage of the module. This is accomplished by an external resistive divider connected across thesequencing voltage before itis fed to the SEQ pin as shown. In addition, a small capacitor (suggested value100pF) should be connected across the lower resistor R2.
For all DLynx modules, the minimum recommended delay between the ON/OFF signal and the sequencing signal is 10ms to ensure that the module output is ramped up according to the sequencing signal. This ensures that the module soft-start routine is completed before the sequencing signal is allowed to ramp up.



The module's output can track the SEQ pin signal with slopes of up to 0.5V/msec during power-up or power-down.To initiate simultaneous shutdown of the modules, the SEQ pin voltage is lowered in a controlled manner. The output voltage of the modules tracks the voltages below their set-point voltages on a one-to-one basis. A valid input voltage must be maintained until the tracking and output voltages reach ground potential.

Synchronization

The module switching frequency can be synchronized to a signal with an external frequency within a specified range. Synchronization can be done by using the external signal applied to the SYNC pin of the module with the converter being synchronized by the rising edge of the external signal. The Electrical Specifications table specifies the requirements of the external SYNC signal. If the SYNC pin is not used, the module should free run at the default switching frequency. If synchronization is not being used, connect the SYNC pin to GND.

PMBus Addressing

The power module can be addressed through the PMBus using a device address. The module has 64 possible addresses (0 to 63 in decimal) which can be set using resistors connected from the ADDRO and ADDR1 pins to SIG_GND. Note that some of these addresses (0, 1, 2,3, 4,5,6,7, 8,9, 10, 11 12,40,44, 45, 55 in decimal)are reserved according to the SMBus specifications and may not be useable. The address is set in the form of two octal (0 to 7)digits, with each pin setting one digit. The ADDR1 pin sets the high order digit and ADDRO sets the low order digit The resistor values suggested for each digit are shown in Table 4(1% tolerance resistors are recommended). Note that if either address resistor value is outside the range specified in Table 4, the module will respond to address 127.

Table 4

Number	0	1	2	3	4	5	6	7
Resistor KΩ	10	15.4	23.7	36.5	54.9	84.5	130	200

PMBus Adjustable Soft Start Rise Time

The soft start rise time can be adjusted in the module via PMBus. When setting this parameter, make sure that the charging current for output capacitors can be delivered by the module in addition to any load current to avoid nuisance tripping of the over current protection circuitry during startup. The TON_RISE command sets the rise time in ms,and allows choosing soft start times between 600us and9ms, with possible values listed in Table 5. Note that the exponent is fixed at -4 (decimal) and the upper two bits of the mantissa are also fixed at 0.

Table 5 Adjustable Rise Time

600μs	900μs	1.2ms	1.8ms	2.7ms	4.2ms	6ms	9ms

PMBus Adjustable Input Undervoltage Lockout

The module allows adjustment of the input under voltage lockout and hysteresis. The command VIN_ON allows setting the input voltage turn on threshold, while the VIN_OFF command sets the input voltage turn off threshold. For the VIN_ON command, possible values are 2.75V, and 3V to 14Vin 0.5V steps. For the VIN_OFF command, possible values are2.5Vto 14Vin 0.5V steps. If other values are entered for either command, they will be mapped to the closest of the allowed values.
VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON results in the new value being rejected,SMBALERT being asserted along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML
Both the VIN_ON and VIN_OFF commands use the "Linear"format with two data bytes. The upper five bits represent the exponent (fixed at -2) and the remaining 11 bits represent the mantissa. For the mantissa, the four most significant bits are fixed at 0.

POWER GOOD

The module provides a Power Good (PGOOD) signal that is implemented with an open-drain output to indicate that the output voltage is within the regulation limits of the power module. The PGOOD signal will be de-asserted to a low state if any condition such as over temperature, over current or loss of regulation occurs that would result in the output voltage going outside the specified thresholds. The PGOOD thresholds are user selectable via the PMBus (the default values are as shown in the Feature Specifications Sectionl.Each threshold is set up symmetrically above and below the nominal value. The POWER_G00D_ON command sets the output voltage level above which PGOOD is asserted lower threshold). For example, with a 1.2V nominal output voltage,the POWER_GOOD_ON threshold can set the lower threshold to 1.14 or 1.1V. Doing this will automatically set the upper thresholds to 1.26 or 1.3V.

Notes

① The converter case is not a hermetically-sealed construction, a sufficient drying process is required after the converter cleaning, make sure the liquid congregated is removed, or it will damage the converter or degradation of performance. Recommend to clear the appearance of the converter with alcohol.
② Input voltage range is wide.If the impedance of input source is high, ensure that the supply voltage is not lower than 3Vdc， When the input inductive resistance is large, the appropriate filter capacitor should be added near the converter input pin for impedance matching.
③ Long-time soldering pins may cause internal connections loose，and duration shall not exceed 5s.
④ Please contact us for more detailed information.

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